BOE	PRODUCT GROUP	REV	ISSUE DATE
	Customer SPEC	Rev. PO	July.f6,2f'

TITLE :QVf85FHB−N8f
Product Specification
Rev. PO

Customer		Recipient's recognition	
Take charge		Establishment	MR.HO
Audit		Audit	
Approved		Approved	

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REVISION HISTORY

(●)preliminary specification

(   )Final specification

Revision No.	Page	Description of changes	Date	Prepared
Rev.O		Initial Release	July.f6,2f'	MR.HO

f.O GENERAL DESCRIPTION

f.f Introduction

QVf85FHB−N8f is a color active matrix TFT LCD MDL using amorphous silicon TFT's
  (Thin Film Transistors) as an active switching devices. This Open Cell has a f8.5 inch diagonally measured active area with FHD resolutions (f920 horizontal by f080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display f6.7M colors. The TFT−LCD panel is adapted for a low reflection and higher color type.
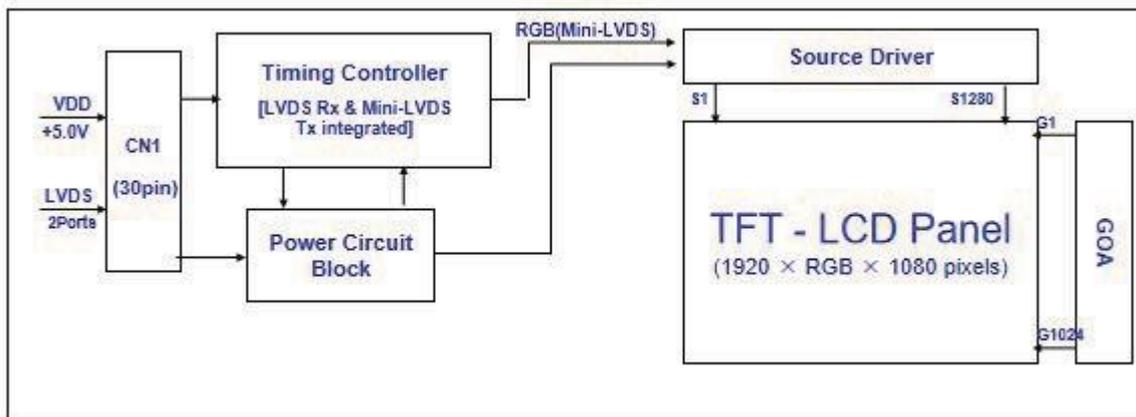
f.2 Features
    .LVDS interface with 2 pixel ʃ clock
  .High−speed response
  .Low color shift image quality
.8−bit color depth, display f6.7M colors
    Wide viewing angle
    DE (Data Enable) only mode
    HADS technology is applied for high display quality
    RoHS compliant

f.3 Application

Commercial Digital Display

Display Terminals for Control System

Landscape and Portrait   Display

f.4 General Information

| Parameter	Specification	Unit	Remarks
Active area	4O8.96 (H) * 23O.O4 (V)	MM	
Number of pixels	f92O(H) ×fO8O(V)	pixels	
Pixel pitch	2f3(H) x 2f3(V)	MM	
Pixel arrangement	Pixels RGB Vertical stripe		
BLU Brightncs	5OO	Cdf Î	
Display colors	f6.7M	colors	
Display mode	Normally Black		
Dimensional outline	43O.4(H) × 254.6(V) × 9.5(D) typ.		
Sealing Area	6.69f5f6.62f6.62	mm	UfDfLfR
Surface Treatment	Haze : 25%		
Back−light	f-LED Lighting Bar type		

2.O ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non–operational maximum voltage and current values are listed in Table 2

< Table 2. Absolute Maximum Ratings>

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V DD	–0.3	5.5	V	Ta = 25 ?
Logic Supply Voltage	V IN	VSS–O.3	V DD +O.3	V	
Operating Temperature	T OP	0	5O	?	f)
Storage Temperature	T ST	–20	6O	?	f)
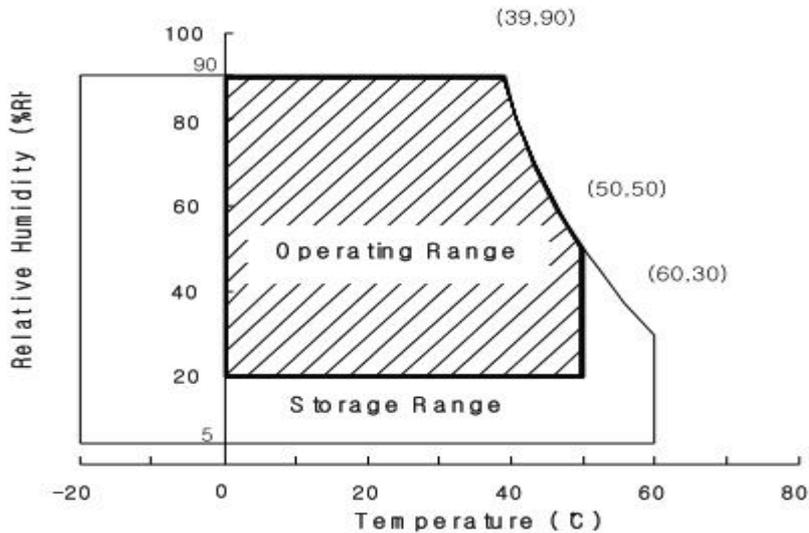
3. Electrical Specifications

3.f Open Cell Power Consumption (TA = 25 ± 2 °C)

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V DD	4.5	5.O	5.5	V	Notef
Power Supply Current	I DD	-	5OO	72O	MA	
In−Rush Current	I RUSH	-	2.O	3.0	A	Note2
Permissible Input Ripple Voltage	V RF	-	-	300	MV	Notef,3
High Level Differential Input Threshold Voltage	V IH	-	-	fOO	MV	
Low Level Differential Input Threshold Voltage	V IL	−fOO	-	-	MV	
Differential input voltage	|V ID |	2OO	-	600	MV	
Differential input common mode voltage	Vcm	f.O	f.2	f.5		V IH =f00mV, V IL =−fOOmV
Power Consumption	PD	-	2.5	3.6	W	

Notes : f. The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VDD=5.OV, Frame rate=6OHz

Clock frequency 75.4MHz. Test Pattern of power supply current

a) Typ : Color Test

b) Max : Skip Sub−pixel

2. Duration of rush current is about 2 ms and rising time of VDD is 52O µs ± 2O %

3. Ripple Voltage should be covered by Input voltage Spec.

4.O OPTICAL SPECIfiCATION

4.f Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance   f lux and temperature =
25   2 $\degree$?) with the equipment of Luminance meter system (Goniometer system and TOPCONE PR73O) and test unit shall
be located at an approximate distance 5Ocm from the LCD surface at a viewing angle of 0 and 8 equal to O   . We refer
to 0 Ø=O (=0 3) as the 3 o'clock direction (the "right"), 0 Ø=9O (= 0 f2) as the f2 o'clock direction ("upward"), 0 Ø=f8O (= 0 9
) as the 9 o'clock direction ("left") and 0 Ø=27O (= 0 6) as the 6 o'clock direction ("bottom"). While scanning 0 andfor Ø,
the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 3O
minutes warm–up period. VDD shall be 5.OV +f–fO% at 25 C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

[VDD = 5.OV, Frame rate = 6OHz, Clock = 74.25MHz, Ta =25 $\pm$ 2 ?]

< Table 5. Module Optical >

5.O INTERfACE CONNECTION.

5.f Electrical Interface Connection

● CNf Module Side Connector : UJU ISfOO–L3OR–C23or Equivalent

User Side Connector : JAE FI–X3OH or Equivalent

8 ƒ f8

5.2 LVDS InterGace (Tx; THC63LVDf83A or Equivalent)

5.2.f LVDS Interface

| Pin No	Symbol	Description	Pin No	Symbol	Description
1	RXO0-	Negative Transmission data of Pixel 0 (ODD)	16	RXE1+	Positive Transmission data of Pixel 1 (EVEN)
2	RXO0+	Positive Transmission data of Pixel 0 (ODD)	17	GNG	Power Ground
3	RXO1-	Negative Transmission data of Pixel 1 (ODD)	18	RXE2-	Negative Transmission data of Pixel 2 (EVEN)
4	RXO1+	Positive Transmission data of Pixel 1 (ODD)	19	RXE2+	Positive Transmission data of Pixel 2 (EVEN)
5	RXO2-	Negative Transmission data of Pixel 2 (ODD)	20	RXEC-	Negative Transmission Clock (EVEN)
6	RXO2+	Positive Transmission data of Pixel 2 (ODD)	21	RXEC+	Positive Transmission Clock (EVEN)
7	GND	Power Ground	22	RXE3-	Negative Transmission data of Pixel 3 (EVEN)
8	RXOC-	Negative Transmission Clock (ODD)	23	RXE3+	Positive Transmission data of Pixel 3 (EVEN)
9	RXOC+	Positive Transmission Clock (ODD)	24	GND	Power Ground
10	RXO3-	Negative Transmission data of Pixel 3 (ODD)	25	NC	No. Connection
11	RXO3+	Positive Transmission data of Pixel 3 (ODD)	26	NC	No. Connection
12	RXE0-	Negative Transmission data of Pixel 0 (EVEN)	27	NC	No. Connection
13	RXE0+	Positive Transmission data of Pixel 0 (EVEN)	28	VDD	
14	GND	Power Ground	29	VDD	Power Supply: +5V
15	RXE1-	Negative Transmission data of Pixel 1 (EVEN)	30	VDD	

Note : Pin 24 should be connected with GND.
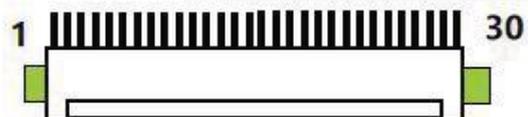
5.2.2 LVDS Rx Interface Timing Parameter

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCP	14.8	18.5	22.2	nsec	
Receiver Data Input Margin	tRMG	-0.35	-	0.35	nsec	fCLKIN=110MHz
		-0.40	-	0.40	nsec	fCLKIN=95MHz
		-0.45	-	0.45	nsec	fCLKIN=85MHz
		-0.60	-	0.60	nsec	fCLKIN=65MHz
Input Data 0	tRIP1	- | tRMG |	0.0	| tRMG |	Clock	
Input Data 1	tRIP0	T/7- | tRMG |	T/7	T/7+ | tRMG |	Clock	
Input Data 2	tRIP6	2 T/7- | tRMG |	2T/7	2T/7+ | tRMG |	Clock	
Input Data 3	tRIP5	3T/7- | tRMG |	3T/7	3T/7+ | tRMG |	Clock	
Input Data 4	tRIP4	4T/7- | tRMG |	4T/7	4T/7+ | tRMG |	Clock	
Input Data 5	tRIP3	5T/7- | tRMG |	5T/7	5T/7+ | tRMG |	Clock	
Input Data 6	tRIP2	6T/7- | tRMG |	6T/7	6T/7+ | tRMG |	Clock	
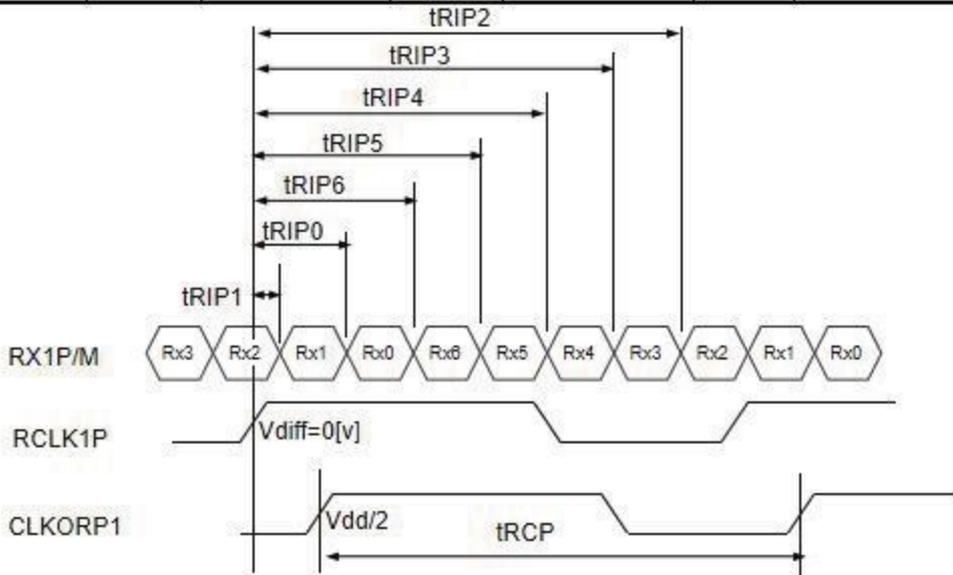
* Vdiff = (RXz+)-(RXz-),.... ,(RXCLK+)-(RXCLK-)

5.2.3 SIGNAL TIMING SPECIFICATION

	Item	Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	60	74.25	78	MHz
	High Time	Tch	-	4/7Tc	-	
	Low Time	Tcl	-	3/7Tc	-	
Frame Period		Tv	1100	1125	1149	lines
			48.5	60	63	Hz
Horizontal Active Display Term	Valid	t_{HV}	-	960	-	t_{CLK}
	Total	t_{HP}	1060	1100	1200	t_{CLK}
Vertical Active Display Term	Valid	t_W	-	1080	-	t_{HP}
	Total	t_{VP}	1100	1125	1149	t_{HP}

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	60	74.25	78	MHz
T_{LVSK}	LVDS channel to channel skew	F=100MHz V_{IC}=1.2V V_{ID}= ± 400mV	-380	-	+380	ps
F_{LVMOD}	Modulating frequency of input clock during SSC		60	-	85	KHz
F_{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T_{CY-CY}	Cycle to Cycle jitter		-	-	100	ps

6.O Backlight Unit

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Light Bar Input Voltage Per Input Pin	VPIN	-	36	42	V	Duty fOO%
LED Light Bar Input Current Per Input Pin	IPIN	8O	8O	8O	MA	Notef,2,
LED Power Consumption	P BL	-	ff.52	f3.44	W	Note 3
LED Life−Time	-	30000			Hrs	Note 4

LED bar consists of52LED packages,4 strings(parallel)*f3packages(serial)

Notef: There are One light bar ,and the specified current is input LED chip fOO% duty current

Note2: The sense current of each input pin is 8OmA

Note3: P BL =4 Input pins*VPIN ×IPIN

Note4: The lifetime is determined as the time at which luminance of LED become 5O% of the initial brightness or not normal lighting at IPIN=8OmA on condition of continuous operating at

25 $\pm$2 ?
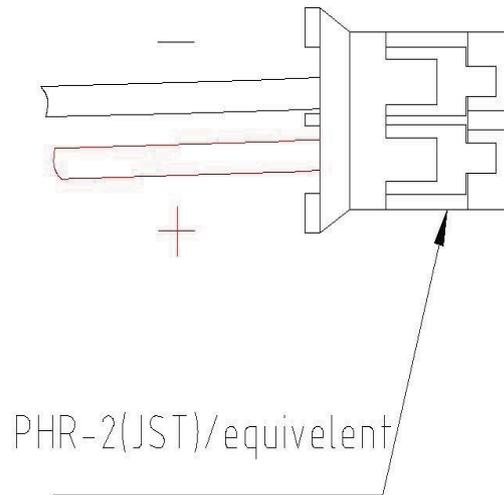
Lightbar Circuit

01   13
14   26
27   39
40   52

13Series，4Parallels

PHR-2(JST)/equivelent

F.0 APPENDIX

Figure f. Measurement Set Up
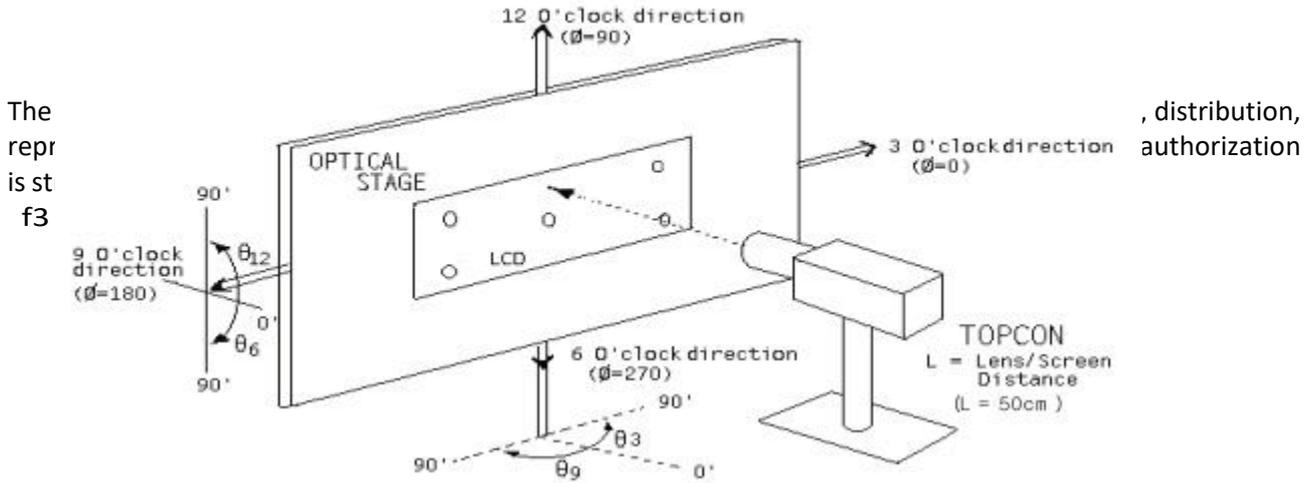
Figure 2. White Luminance and Uniformity Measurement Locations (9 points)

Figure 3. Response Time Testing

The ... re, distribution, repr ... or authorization is st ... f4

Figure 4. Cross Modulation Test Description
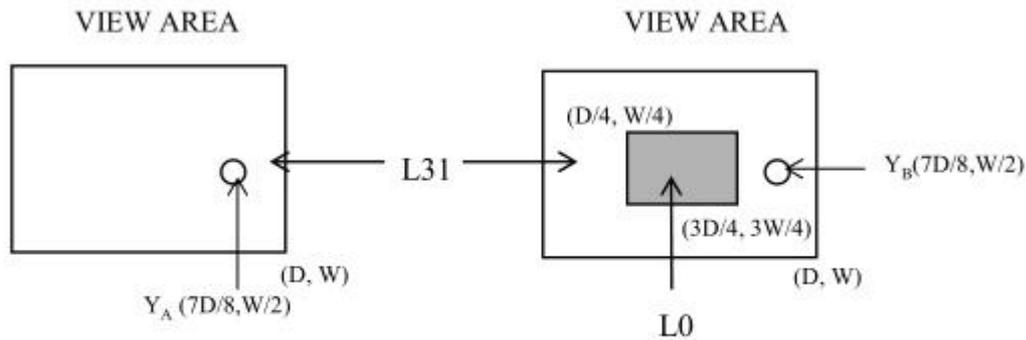
$$\text{Cross-Talk } (\%) = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Where: Y_A = Initial luminance of measured area (cdfm 2)

Y_B = Subsequent luminance of measured area (cdfm 2)

The location measured will be exactly the same in both patterns

Figure 5. TFT−LCD Module Outline Dimensions (Front view)
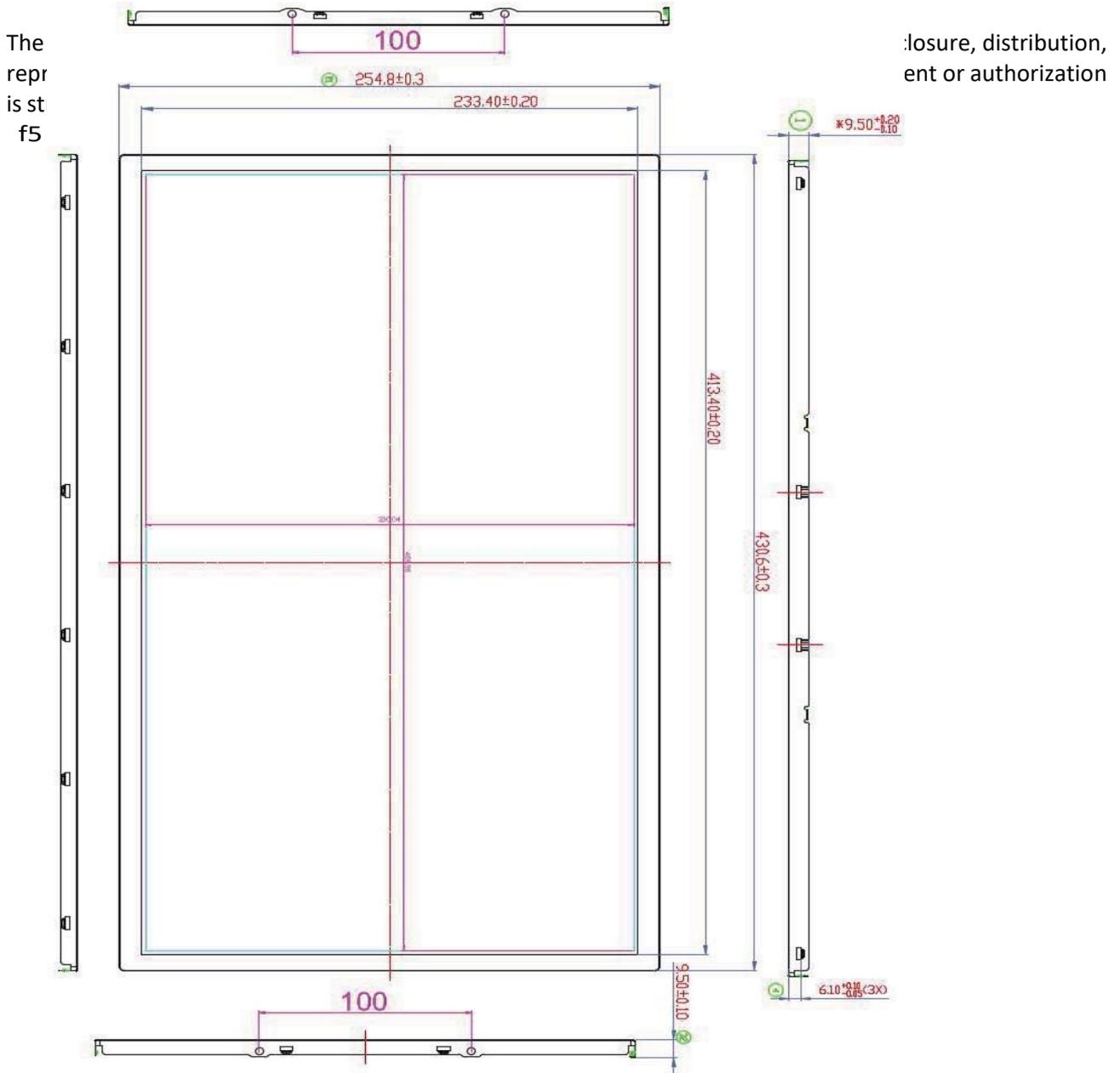
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Figure 6. TFT−LCD Module Outline Dimensions (Rear view)
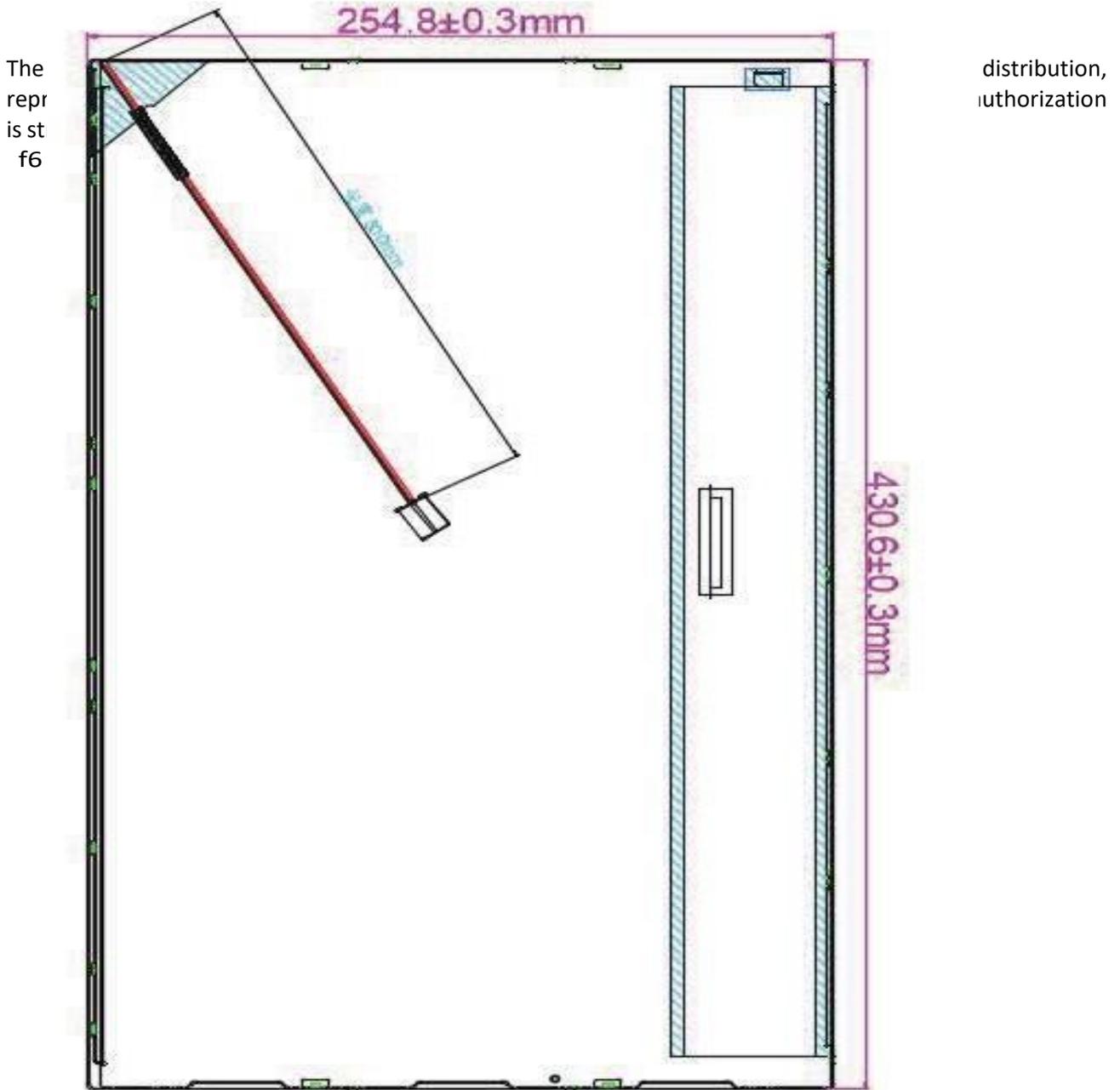
8.O Packing

8.f Packing Order

6箱/层/每箱10PCS
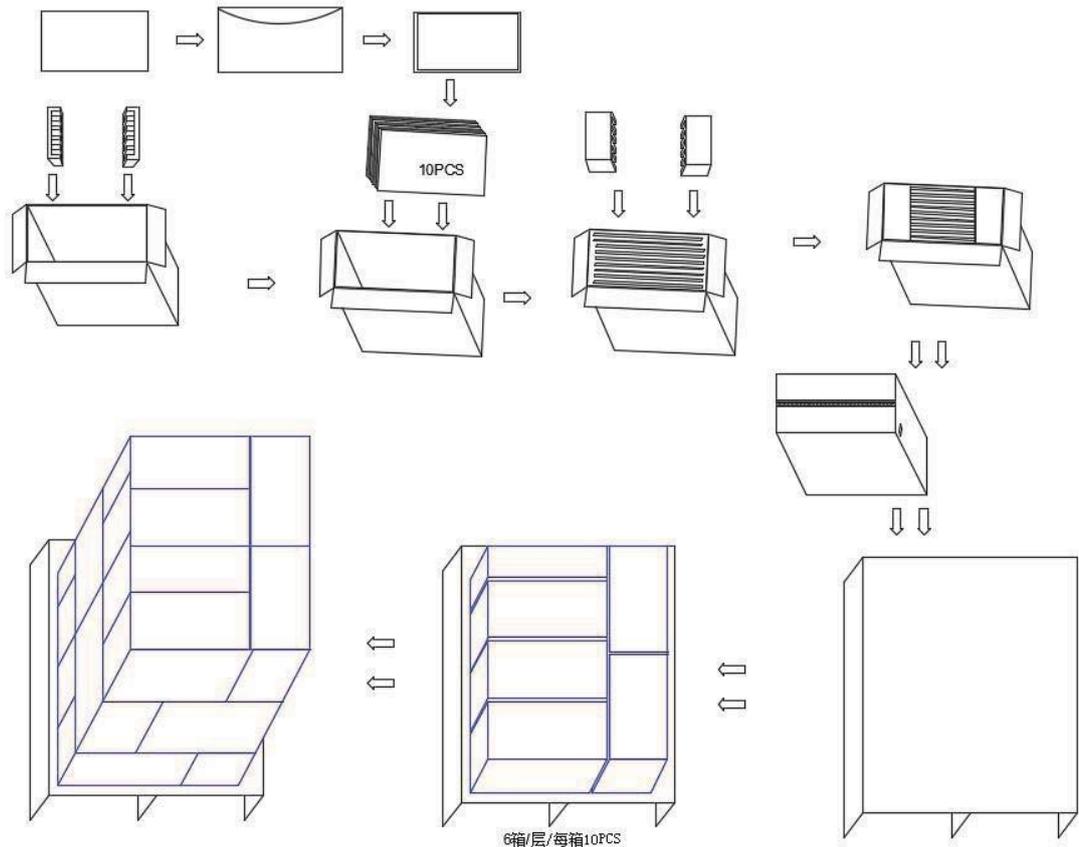
9.OGeneral Precautions

9.1Storage

f. Stor the module ina dark room where must keep at 25 ± 10?, Ç$\pm10\%$RH, the module ›hall
   be e✕po›ed under ›trong light ›uch a› direct ›unlight.

². Do not ›tore the produce in ›urrounding› containing organic ›olvent or corro›ive
ga›

3. Store the module in an anti–electro›tatic container or £ilm.

9.2 Handing
1. Do not ›ubject the module to mechanical ›hock or to e✕ce››ive £orce
     On it› ›ur£ace
². To avoid contamination on the di›play ›ur£ace, do not touch the module
     Sur£ace with bare hand›
3. Wu›t be the correct way to connec the power cable,otherwi›e it will
     Cau›e damage
  9.3 tran›portation
    1. In tran›porting,Good› are ›trictly prohibited during the ultra‐high ›tacking
       E✕tru›ion,up›ide down,entire vehicle liading and unloading.
  ². Per›on› who handle the module ›hould be grounded through adequate method›.
  9.4 Other
  1. About thi› ›peci£ication,i£ any que›tion,go through both ›ide› agreement Po›t‐
       proce››ing.
  ². Any change› mu›t get into contant with each other,get tht agreement then
       To change ,and update the content› to record.